清华大学工程物理系
Department of Engineering Physics Tsinghua University

Development of CMOS CSA for Point Contact HPGe Detectors

Zhi Deng for HPGe detector group @
Department of Engineering Physics, Tsinghua University

Application of Germanium Detector in Fundamental Research
Beijing, March 23-29, 2011

Outlines

- Introduction
- CMOS CSA Design
  - Noise Optimization
  - Reset
- Test Results
- Summary & Future Plan

Introduction

- ULE HPGe Detector

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New limits on spin-independent and spin-dependent couplings of low-mass WIMP dark matter with a germanium detector at a threshold of 220 eV

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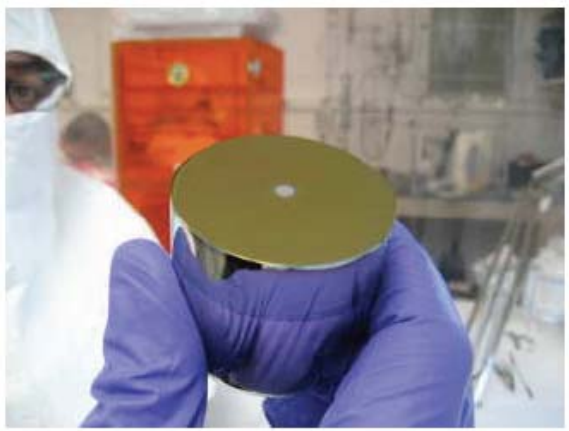
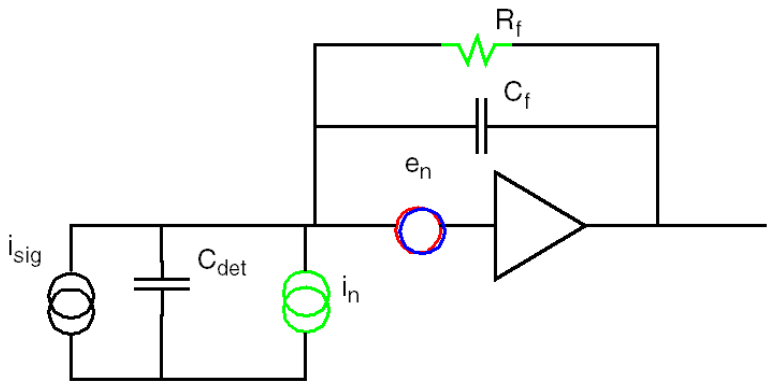
Point-contact HPGe, ~1pF



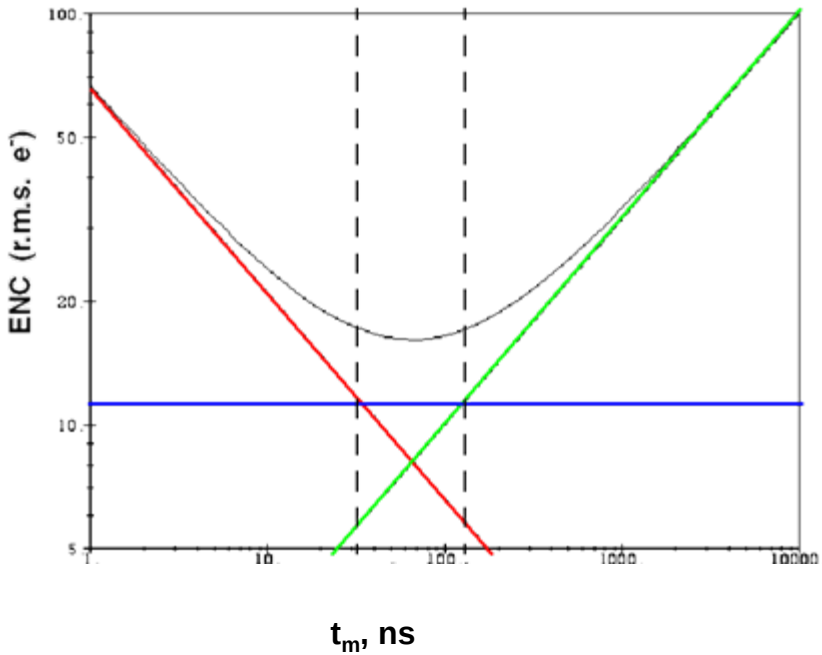
The key technologies for lowering the energy threshold is using small capacitance detector and ultra low noise readout

- JFET vs. CMOS for small capacitance detectors



$$C_{tot} = C_{\det} + C_{in}$$

$$ENC^2 = \frac{a_1 e_{nw}^2 C_{tot}^2}{\tau} + a_2 K_F C_{tot}^2 + a_3 i_n^2 \tau$$



As the detector capacitance goes down, the contribution from 1/f noise become non-dominant anymore!

- What is the limit for 1/f noise

$$ENC_f^2 = a_2 \pi \frac{K_f}{C_g} \left(C_d + C_g \right)^2 \rightarrow$$

$$ENC_{f,opt} \approx \sqrt{2\pi K_f C_d}$$

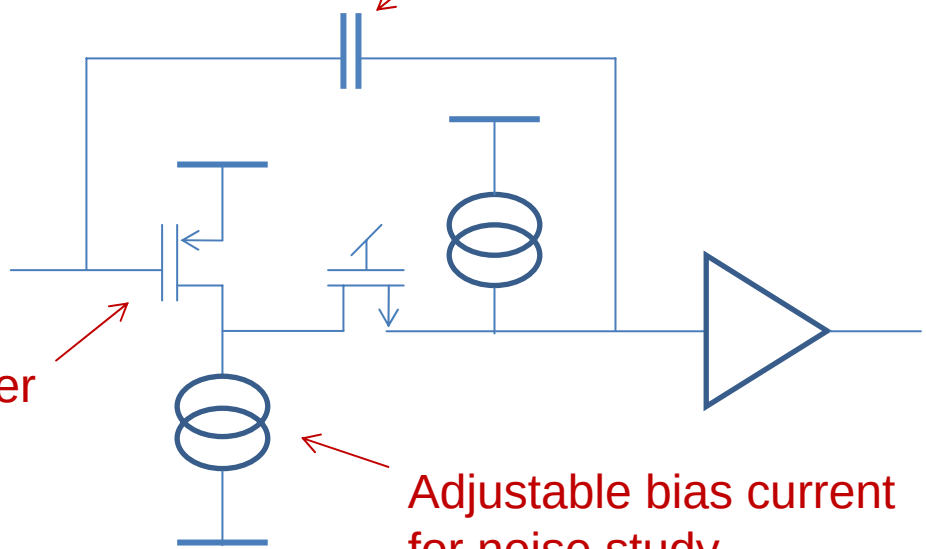
Borrowed from Paul O'Connor's talk in FEE2006

e.g., $K_f = 10^{-25}$J, C_d=1pF ➔ $ENC_f \sim 5\ e^-$

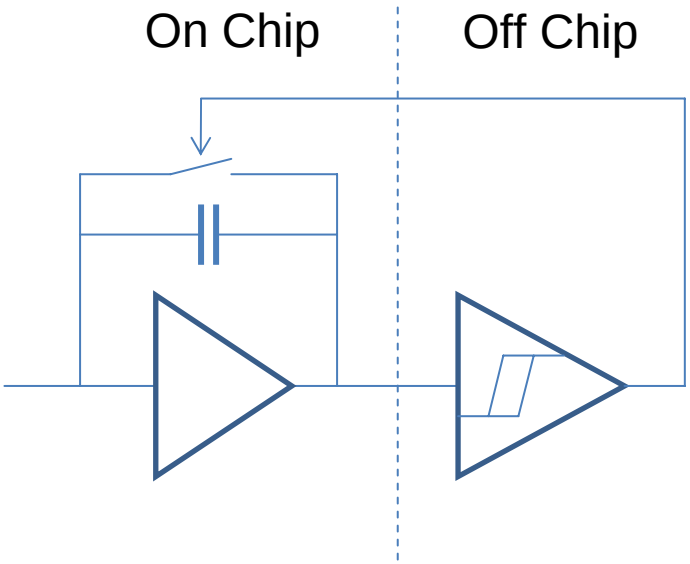
Why not CMOS then?

CMOS CSA Design

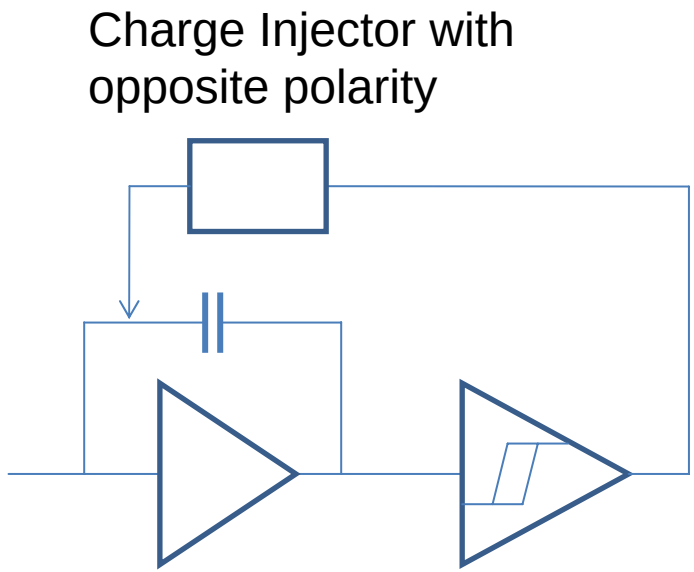
- Noise Optimization



- Reset

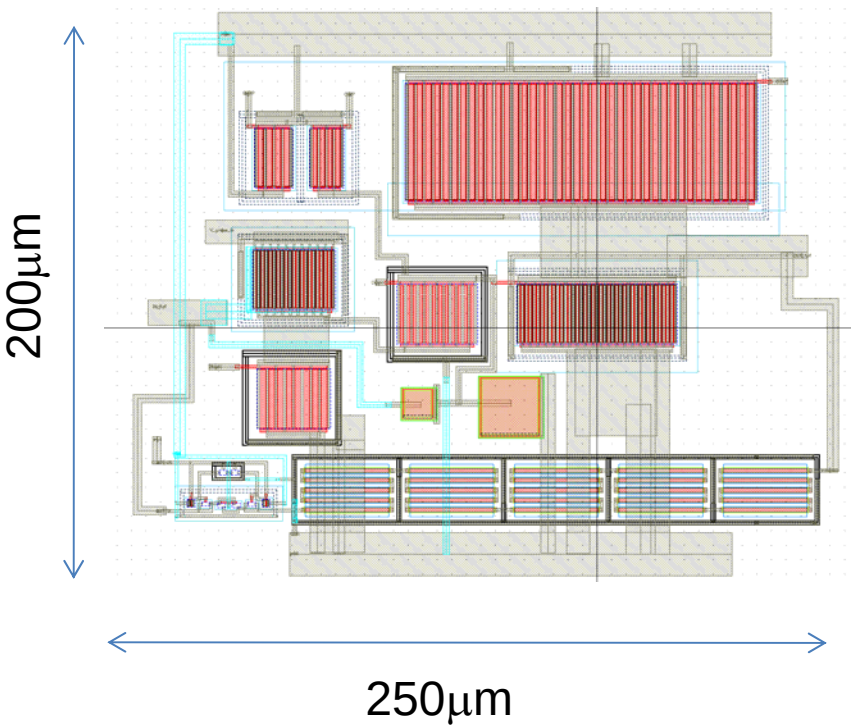


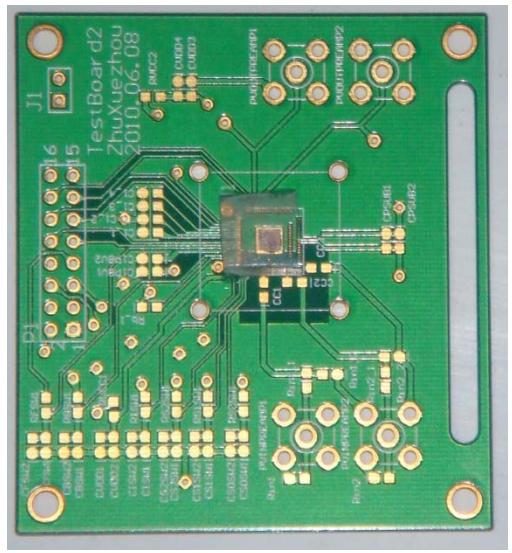
Pulse Reset 1



Pulse Reset 2

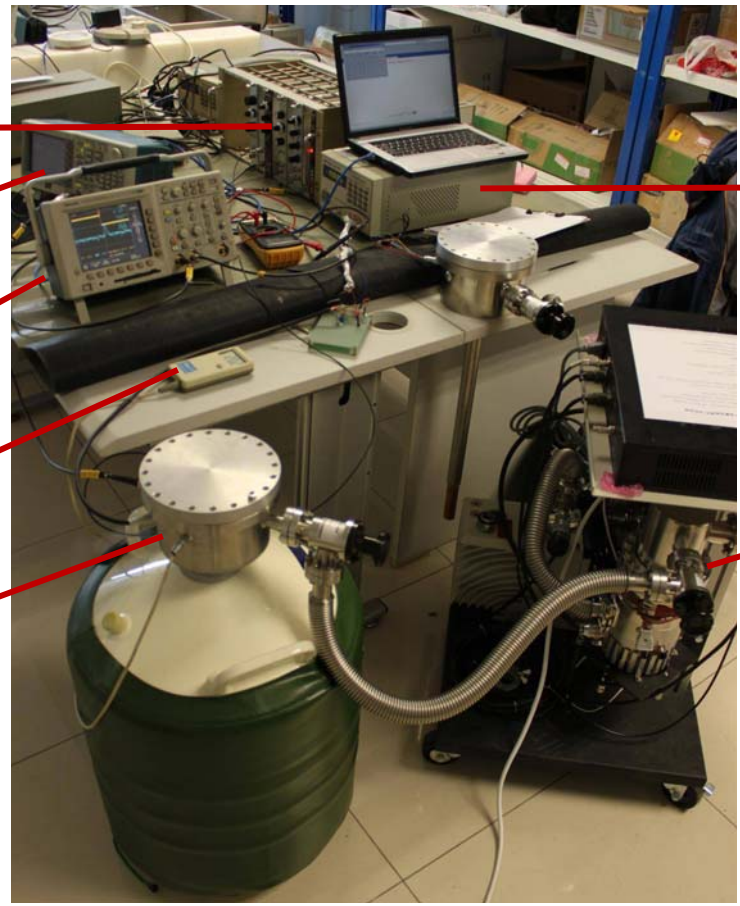
- Layout and test board



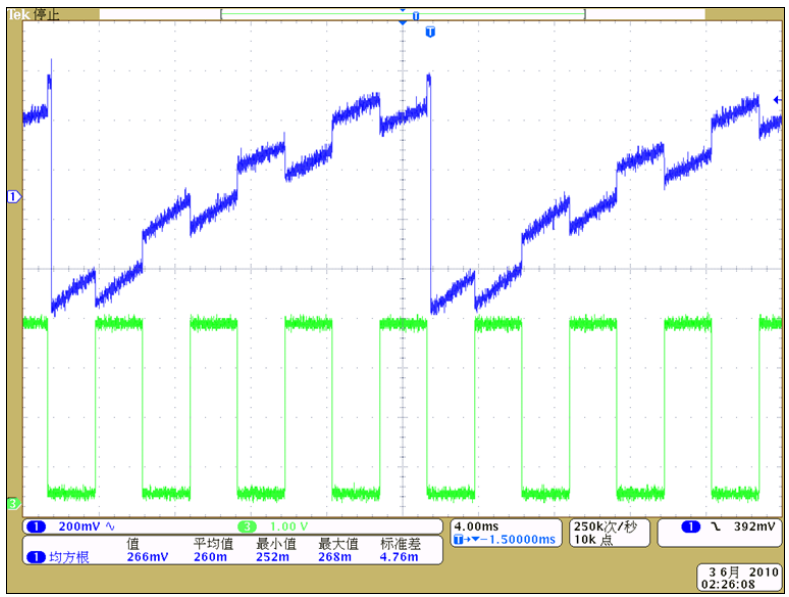


Test Results

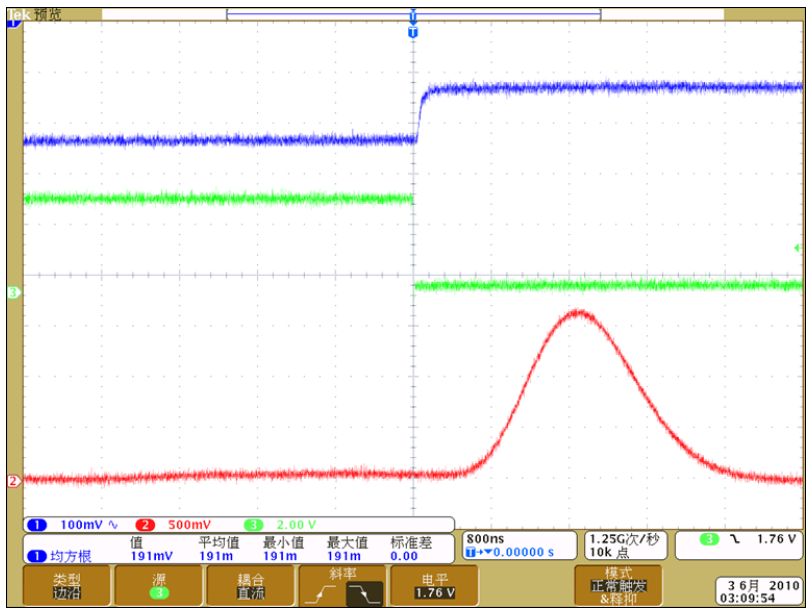
- Test Setup



- Injected with test signals

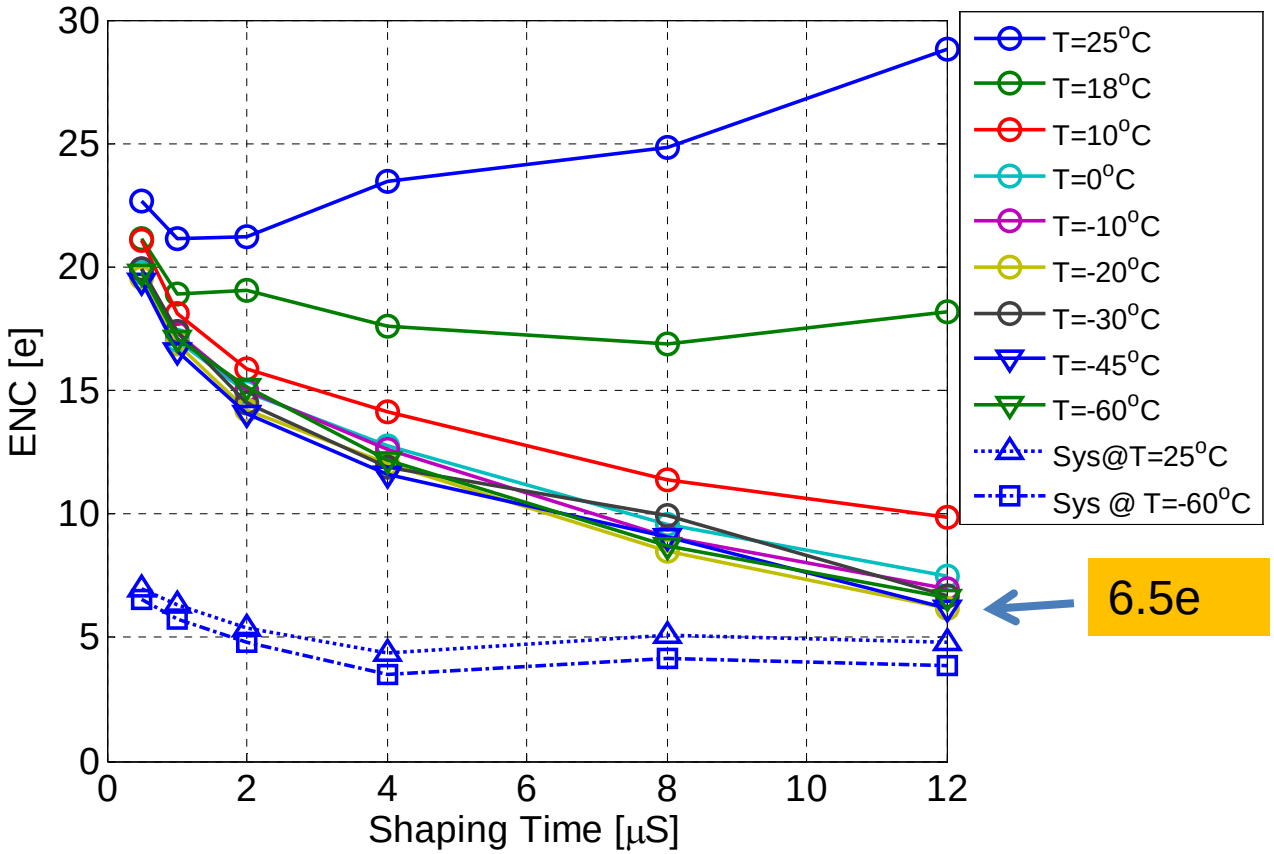


Rise time is about 30ns for 1.5m long cable



After shaper

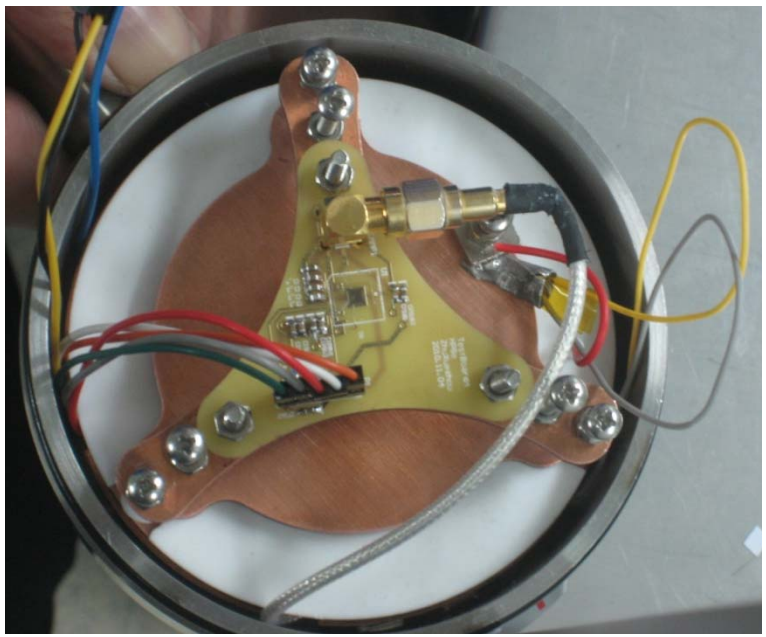
- ENC

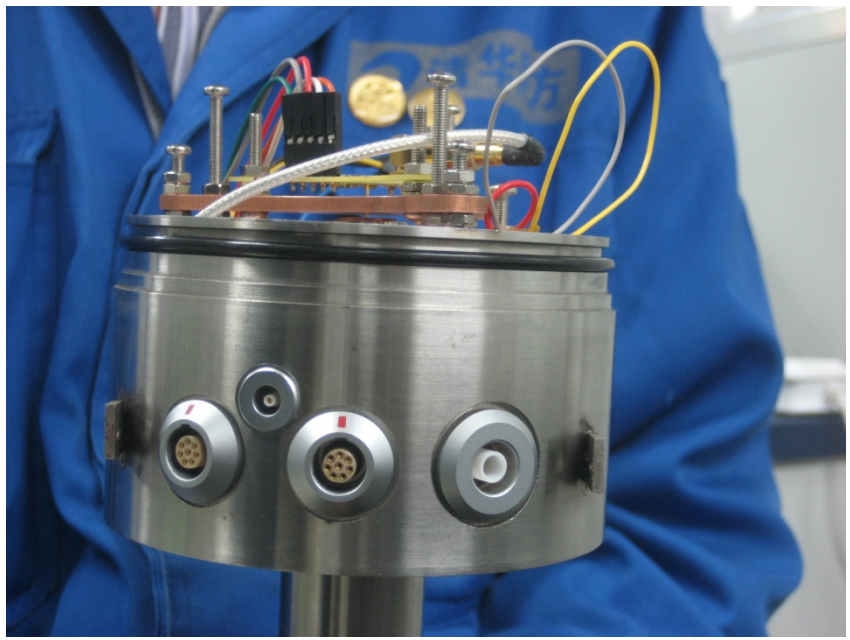

ENC [e]
Shaping Time [μS]
0
5
10
15
20
25
30
0
2
4
6
8
10
12
T=25°C
T=18°C
T=10°C
T=0°C
T=-10°C
T=-20°C
T=-30°C
T=-45°C
T=-60°C
Sys@T=25°C
Sys @ T=-60°C
6.5e

Summary & Future Plan

- A CMOS charge sensitive preamplifier has been designed for point-contact HPGe detectors, with noise optimized for 1pF capacitance. Sub-10e ENC has been achieved without detector. Testing with detector is undergoing.
- A second version chip has been designed and fabricated and it will also be evaluated soon.
- More deep study on cryogenic CMOS transistor model, long term stability…

Thanks





The test setup has been done for the first prototype ASIC with the first prototype of point contact HPGe detector